said substrate to form a source, channel and drain region of said vertical MOS transistor, and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layers surround said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from [and overlying] said alternating N-type and P-type layers by a layer of gate insulating material, said floating gate overlying at least said channel region of said vertical MOS transistor;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate.

REMARKS AS TO CHANGES TO CLAIM 1

Claim 1 was not rejected for indefiniteness. However, some volunatary amendments have been made to improve the precision of description by the claim of the intended structure. The clause "array comprised of a plurality of EEPROM memory cells, each cell" has been removed voluntarily and not in response to any rejection because the claim by its structure is properly directed just to a single nonvolatile memory cell in an array and not the entire array. In line 6 of the claim, the second instance of "layer" has had been made plural to correspond to the actual structure depicted in the drawings so as to not render this portion of the claim indefinite. The phrase "to form a source, channel and drain region of said vertical MOS transistor" to make clear the relationship between the alternative N-type and P-type layers in the substrate and the vertical MOS transistor being formed.

The second element of the claim was amended as follows:

> said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from [and overlying] said alternating N-type and P-type layers by a layer of gate insulating material, said floating gate overlying at least said channel region of said vertical MOS transistor

The word "and overlying" were removed because the floating gate does not necessarily completely overlie the source and drain regions but it will always overlie the channel region. The clause , said floating gate overlying at least said channel region of said vertical MOS transistor was added to clarify that the floating gate must overlie the channel region.

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1. (Clean) A nonvolatile memory cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by alternating N-type and P-type doped layers in said substrate to form a source, channel and drain region of said vertical MOS transistor, and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layers surround said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from said alternating N-type and P-type layers by a layer of gate insulating material, said floating gate overlying at least said channel region of said vertical MOS transistor;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate.

2. (Twice Amended - Version to show changes) A nonvolatile memory cell [array comprised of a plurality of nonvolatile memory cells, each memory cell] comprising:

a semiconductor substrate having a drain region of a first conductivity type formed therein [and having a surface coincident suitable to act as a drain region of a vertical MOS transistor];

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type;

a recessed gate window in the form of a well etched in said semiconductor substrate [through said first layer of insulating material], said well being deep enough to penetrate through said channel region and into said source region such that at least some portion of the side wall [or sidewalls] of said [trench] well are bordered by said source, drain and channel regions;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said channel region;

a word line comprising conductive material deposited so as to extend into said

well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed so as to insulate at least a portion of said word line overlying said well; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at [each] said memory cell but insulated from said word line by said second layer of insulating material.

REMARKS AS TO CHANGES TO CLAIM 2

The preamble of the claim was voluntarily amended to make the claim directed to a single nonvolatile memory cell instead of an entire array.

The clause "and having a surface coincident suitable to act as a drain region of a vertical MOS transistor" from former line 4 of the claim has been removed since it rendered the claim indefinite and is unnecessary.

The source region element at lines 10 and 11 of the claim has been amended to add a missing "said" to make it clear that the last clause in the element is talking about the same source region mentioned in the first part of the claim element.

The phrase "through said first layer of insulating material" was removed from the recessed gate window element because no first layer of insulating material had been mentioned in the claim up to that point.

The following change was made to eliminate an antecedent basis problem with the word "trench" since the recessed gate window was previously referred to as a well:

"such that at least some portion of the side wall [or sidewalls] of said [trench] well are bordered by"

The words "or sidewalls" were removed voluntarily to make the claim more precise since the well only has one sidewall that goes around its entire perimeter.

The second layer of insulating material was amended in the following way to answer the Examiner's indefiniteness rejection indicating uncertainty as to where the secoond layer of insulating material was located:

> a second layer of insulating material formed so as to insulate at least a portion of said word line overlying said well;

This change, coupled with the following italicized language from the bit line claim element make it clear where the second layer of insulating material is located and what its function is:

> a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at [each] said memory cell *but insulated from said word line by said second layer of insulating material.*

The word "each" was voluntarily removed from the claim element to conform the claim language to the change to the preamble to direct the claim to a single nonvolatile memory cell instead of an entire array.

2. (Clean) A nonvolatile memory cell comprising:

a semiconductor substrate having a drain region of a first conductivity type formed therein;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type;

a recessed gate window in the form of a well etched in said semiconductor substrate, said well being deep enough to penetrate through said channel region and into said source region such that at least some portion of the side wall of said well are bordered by said source, drain and channel regions;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said channel region;

a word line comprising conductive material deposited so as to extend into said well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed so as to insulate at least a portion of said word line overlying said well; and

a bit line formed over said surface of said semiconductor substrate so as to make

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contact with at least a portion of said drain region at said memory cell but insulated from said word line by said second layer of insulating material.

3. (Amended-Version to show changes) A nonvolatile memory cell [array comprised of a plurality of EEPROM memory cells, each cell] comprising:

a semiconductor substrate;

a vertical MOS transistor formed by a first layer of N-type conductivity [and having a surface coincident with the surface of said substrate and] forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said substrate and adjacent to and underlying said first layer relative to the surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying at least said [first, second and third layers] second layer and insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed [on] above said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed [on] above the surface of said substrate so as to be in electrical contact with the surface of said first layer [coincident with the surface of said substrate at each cell in said array,]; and

a spacer layer of insulating material insulating said word line [contact] from said bit line [contact].

REMARKS AS TO CHANGES TO CLAIM 3

The phrase "and having a surface coincident with the surface of said substrate and" has been voluntarily removed from the vertical transistor claim element to improve the precision of description of the claimed structure. This was done because of a concern that the word "coincident" might be misconstrued to mean that the surface of the drain region and the surface of the substrate have to be in the same plane which is not true although these two surfaces were in one plane at some point in the manufacturing process.

The words "contact" have been eliminated from the last element of the claim to remove the antecedent basis problem noted by the Examiner in the final rejection indefiniteness rejection since the word line and bit line are simply referred to as a word line and a bit line and not a word line contact or a bit line contact.

The vertical MOS transistor element has been amended as follows:

> said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying <u>at least</u> said [first, second and third layers] <u>second layer</u> and insulated by a layer of gate insulating material from said first, second and third layers;

This amendment was made voluntarily to improve the precision of the description of the claimed structure so as to specify that the floating gate needs to overlie at least the second layer where the channel region is but does not necessarily need to overlie the first or third layers.

The bit line element has been amended as follows:

> a bit line comprising a layer of conductive material formed on the surface of said substrate so as to be in electrical contact with the surface of said first layer [coincident with the surface of said substrate at each cell in

said array],

The purpose of this amendment is to improve the precision of the claim in describing the claimed structure in that the surface of the first layer (the drain region) does not necessarily have to be coincident with the surface of the substrate. Although the surface of the drain region will be a surface of the substrate, as can be seen from Figure 5, the surface of the drain region may be recessed slightly from the rest of the surface of the substrate so the word "coincident" could be interpreted to be indefinite.

The word line and bit line claim elements have been amended voluntarily to remove the word "on" and substitute the word "above" to make the claim more precise in its description of the location of the word line and the bit line since the word "on" might be misconstrued to mean the word line and bit line have to touch the top surface of the substrate at all points which is not true as is apparent from the drawings.

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3. (Clean) A nonvolatile memory cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by a first layer of N-type conductivity forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said substrate and adjacent to and underlying said first layer relative to the surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying at least said second layer and insulated by a layer of gate insulating material from said first, second and third layers;

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a word line comprising a layer of conductive material formed above said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed above the surface of said substrate so as to be in electrical contact with the surface of said first layer; and

a spacer layer of insulating material insulating said word line from said bit line.

4. (Amended-Version to show changes)The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line is formed above said first layer so as to be above the top surface of said substrate and [contact] contacts said first layer at all points that form a top surface of said first layer between [said] spacer layers of the word [line contacts] lines of adjacent memory cells so as to form a bit line which is self aligned to the edge of said spacer layer.

REMARKS AS TO CHANGES TO CLAIM 4

Removal of the words "contacts" was necessary in line 5 of the claim as amended to conform it to the language of amended claim 3 to prevent an antecedent basis problem. The addition of "memory cell is part of an array comprised of rows and columns of adjacent memory cells" was made to specify the environment in which the memory cell operates so that the rest of the claim made sense in terms of how the bit line contacts the first layer in the space between adjacent word lines.

The change "and wherein said bit line is formed above said first layer so as to be above the top surface of said substrate" was made to clearly specify the second difference over the prior art which is that both bit lines and word lines are formed above the substrate and are not subject to the cross-sectional area constriction of the Mori buried bit line and the resulting increase in resistance and lowering of operating speed.

The phrase "so as to form a bit line which is self aligned to the edge of said spacer layer" has been added to the claim to improve the precision of the description of the claimed structure. The important thing about this claim is that it specifies that the bit line does not have to make contact to the drain region through a contact window that

needs to be formed by a mask since this would cause excessive area to be consumed to account for mask misregistration errors when using a mask to photolithographically etch contact windows down to the drain area.

4. (Clean)The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line is formed above said first layer so as to be above the top surface of said substrate and contacts said first layer at all points that form a top surface of said first layer between spacer layers of the word lines of adjacent memory cells.

5. (Amended - Version to show changes) The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line [contact] contacts said first layer at at least some points between said spacer layers of the word [line contacts] lines of adjacent memory cells and runs over the top of [said word line] word lines said bit line has to cross and is insulated [therefrom] from each said word line at the location of each said memory cell by said spacer layer.

REMARKS AS TO CLAIM 5 CHANGES

The changes to lines 1-4 of amended claim 5 track the changes to claim 4 and are made for the same reasons.

The changes:

> and runs over the top of [said word line] word lines said bit line has to cross and is insulated [therefrom] from each said word line at the location of each said memory cell by said spacer layer

were made to improve the precision of the description of the position of the bit line and how it is insulated from each word line it crosses by the spacer layer at each memory cell.

5. (Clean) The apparatus of claim 3 wherein said memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said bit line contacts said first layer at at least some points between said spacer layers of the word lines of adjacent memory cells and runs over the top of word lines said bit line has to cross and is insulated from each said word line at the location of each said memory cell by said spacer layer.

Please add a new claim 6 as follows:

6. A method of forming a vertically oriented EEPROM memory cell transistor comprising the steps of:

in a semiconductor substrate, forming a source layer of a first conductivity type;

forming a channel region of a second conductivity type in said substrate adjacent to said source layer;

forming a drain region of said first conductivity type in said substrate so as to have a top surface;

forming a well in said substrate located and sized so as to extend down through said drain and channel regions and at least partially into said source region;

forming a floating gate insulating layer on the sidewall which defines the perimeter of the volume of space in said substrate removed by said well, and forming an insulating layer at the bottom of said well;

forming a self-aligned, conductive floating gate on the insulating layer covering said sidewall of said trench by anisotropically etching back a layer of conductor formed over said substrate and the vertical walls of said well so as to remove all horizontal portions of said conductor on the top surface of said substrate and the bottom of said well and leave only portions of said conductor on the vertical walls of said well which overlie at least said channel region;

forming an insulating layer to cover said floating gate;

forming a combined word line and control gate of conductive material which extends down into said well far enough to overlie at least said channel region;